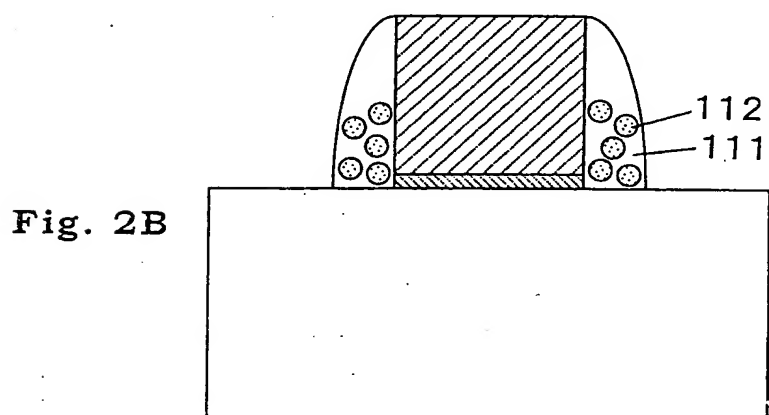
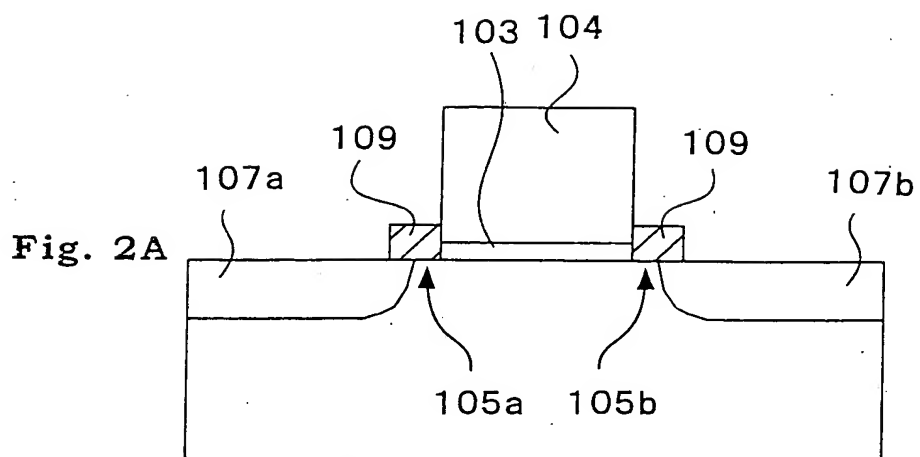
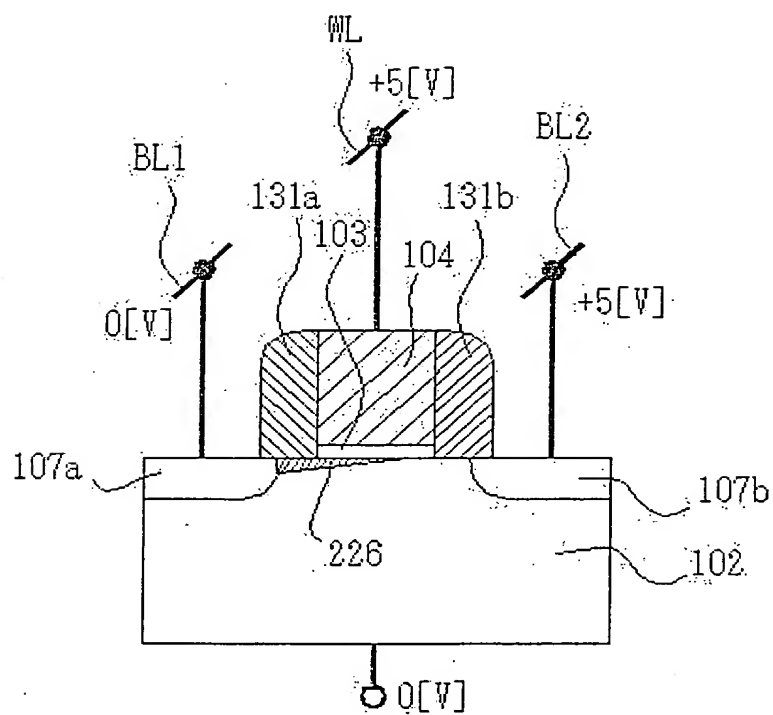


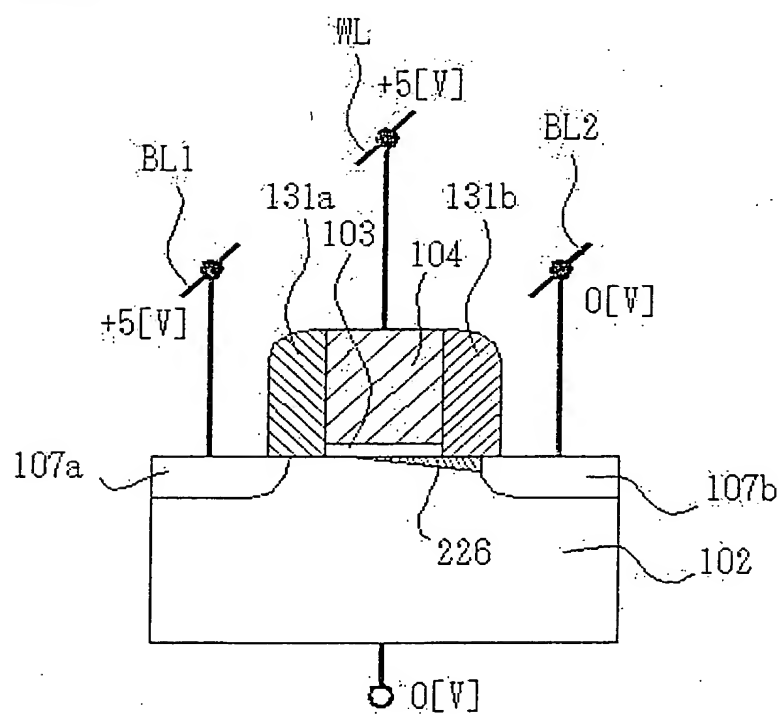
**Fig. 1**



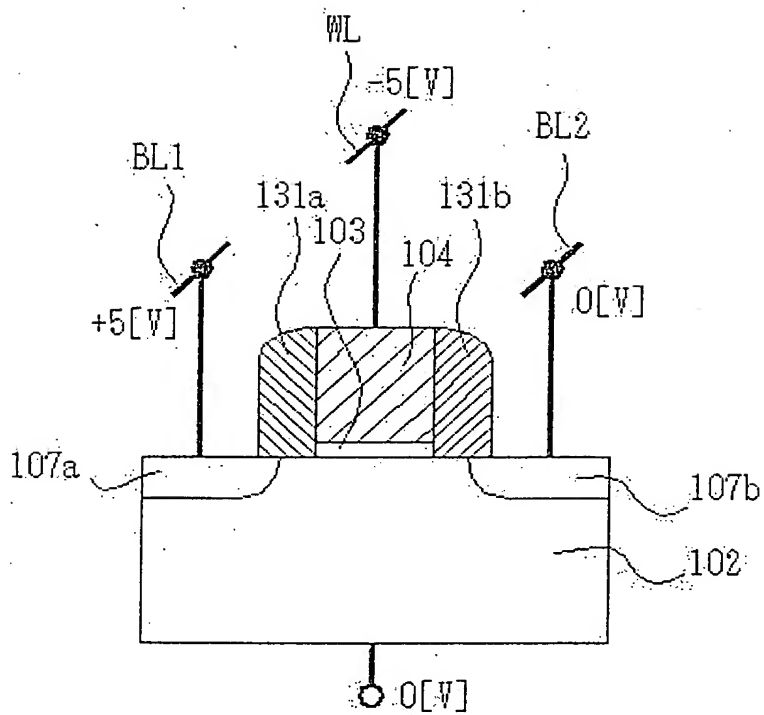
**Fig. 3**



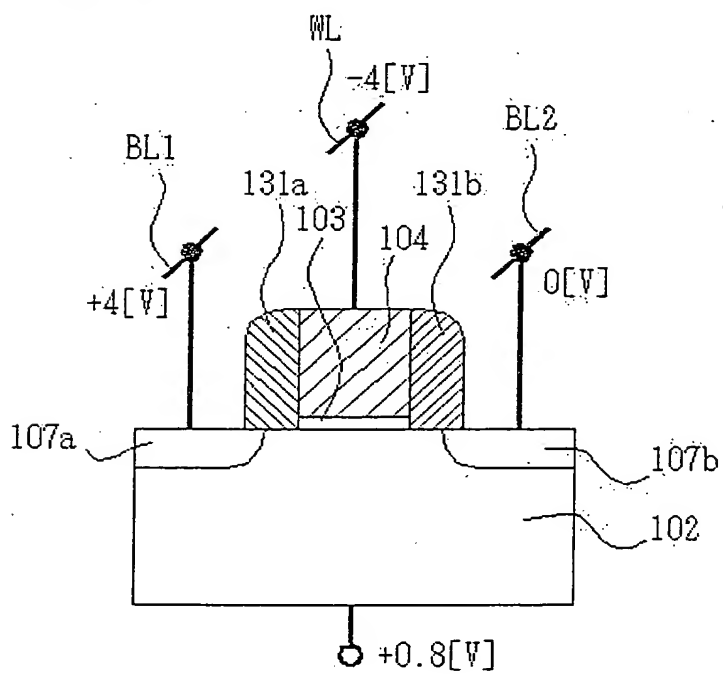
**Fig. 4**



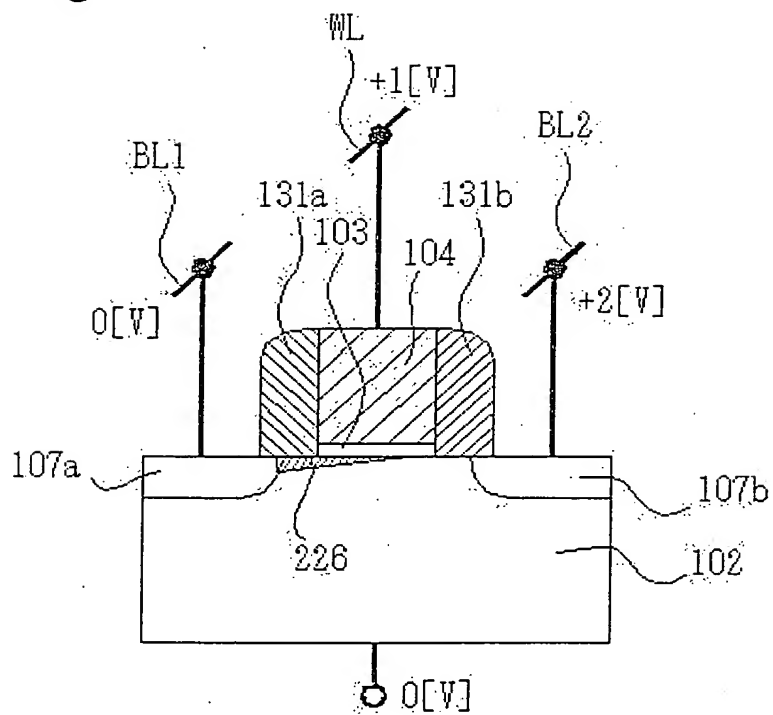
**Fig. 5**



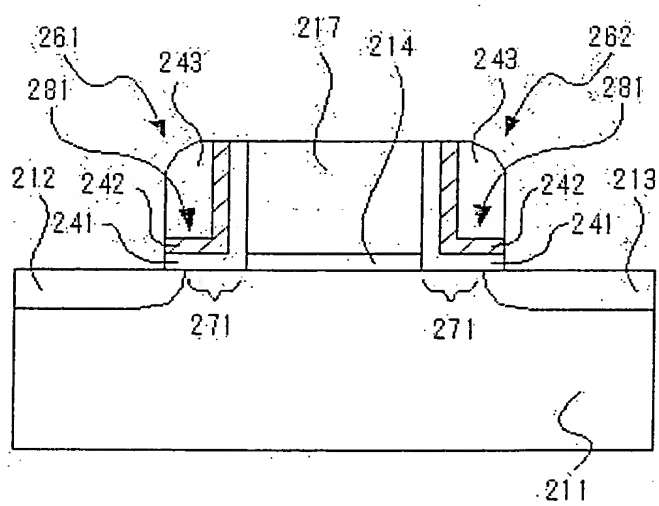
**Fig. 6**



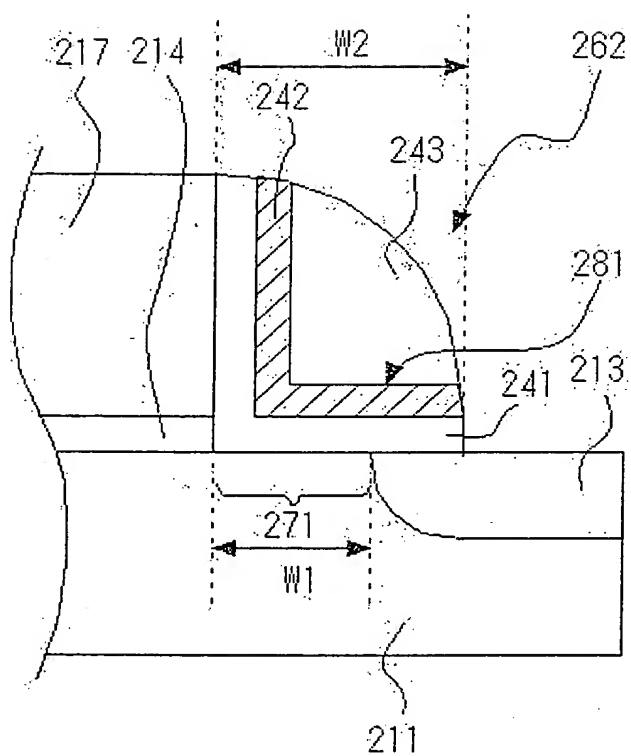
**Fig. 7**



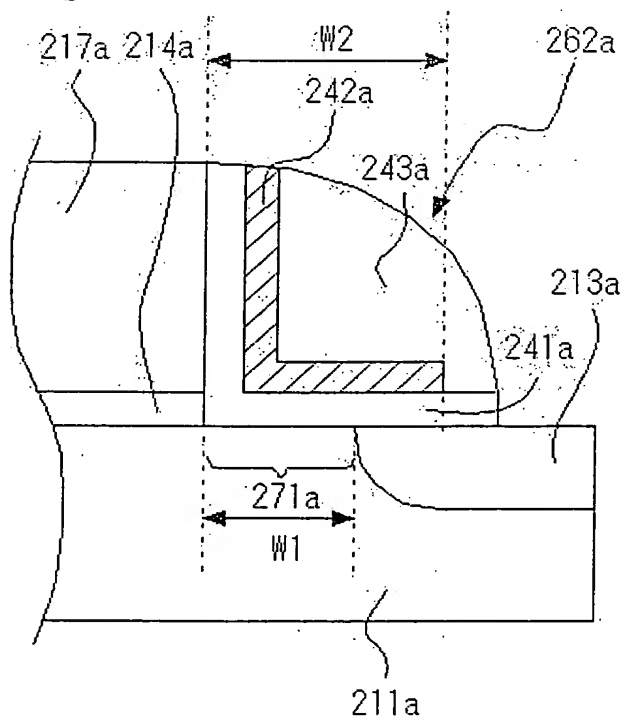
**Fig. 8**



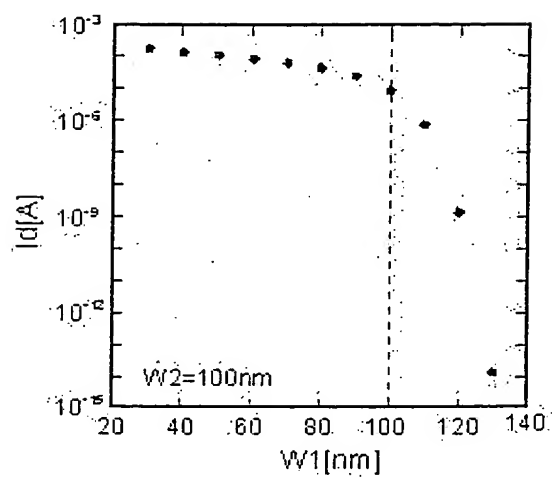
**Fig. 9**



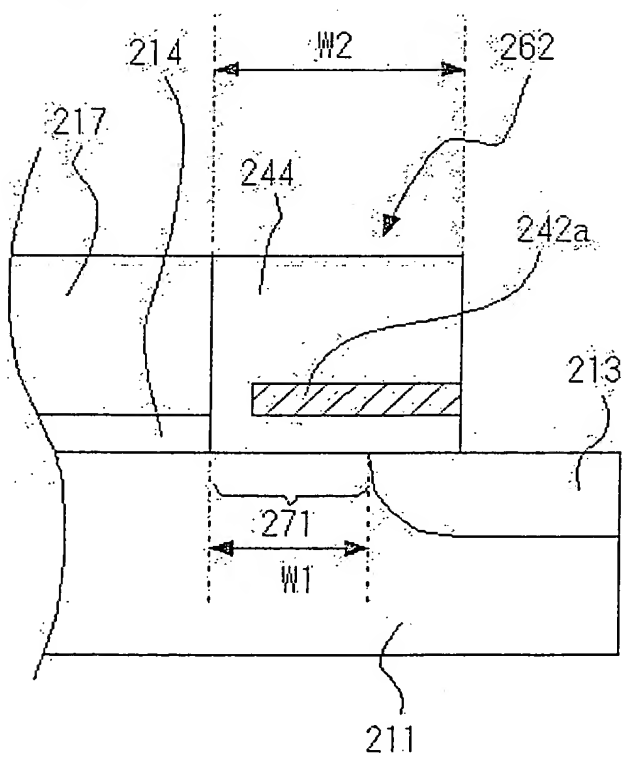
**Fig. 10**



**Fig. 11**



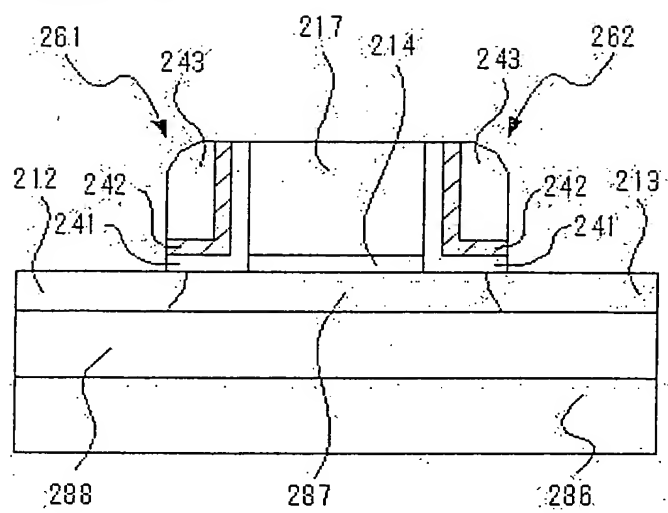
**Fig. 12**



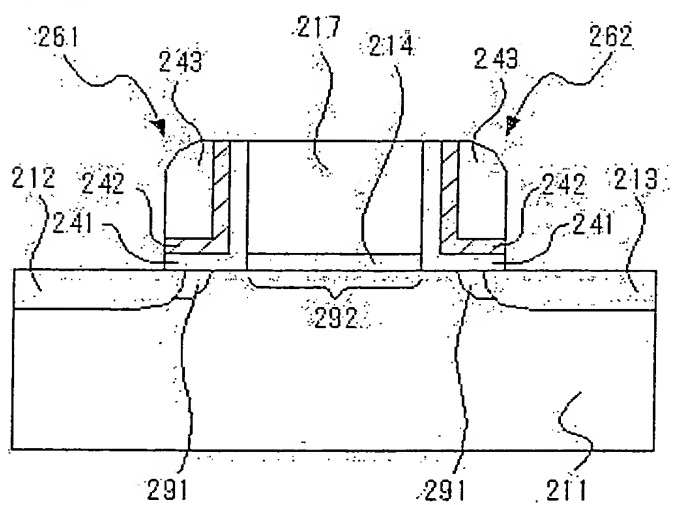
A cross-sectional view of a semiconductor device. A central channel region (217) is flanked by two side regions (214). The side regions are further divided into sub-regions (243) and (242). The channel region is bounded by vertical walls (212, 213). The device is mounted on a substrate (211). Dimensions A, B, and C are indicated. A is the width of the side regions (243), B is the width of the channel region (217), and C is the total width of the device. Other labels include 261, 262, 241, 242, 243, 212, 213, 214, 217, and 271.



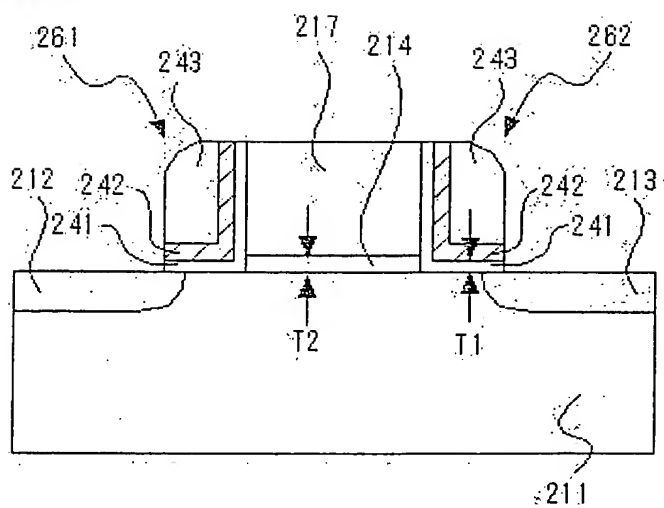
**Fig. 15**



**Fig. 16**



**Fig. 17**



**Fig. 18**

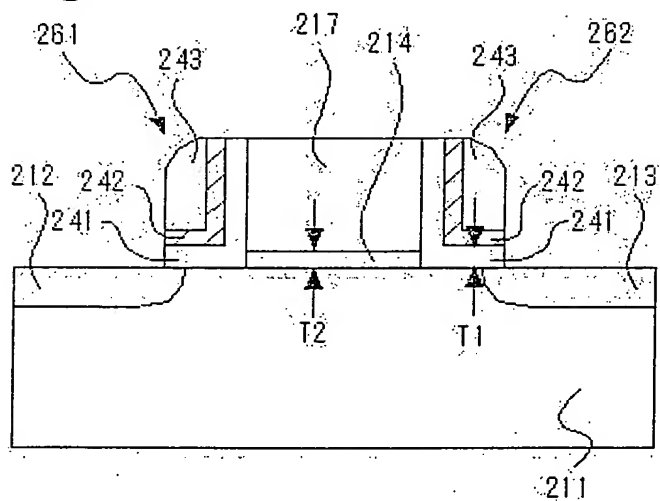


Fig. 19

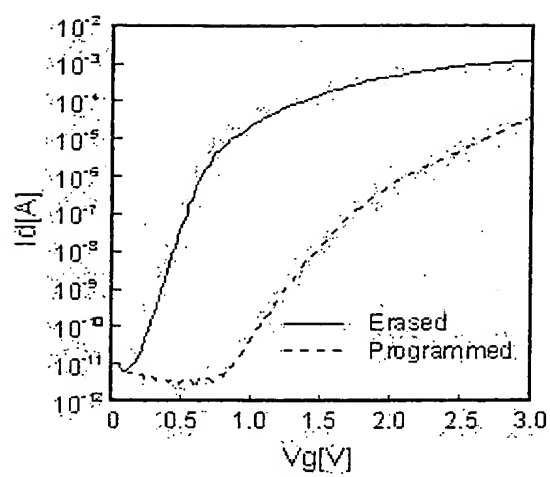
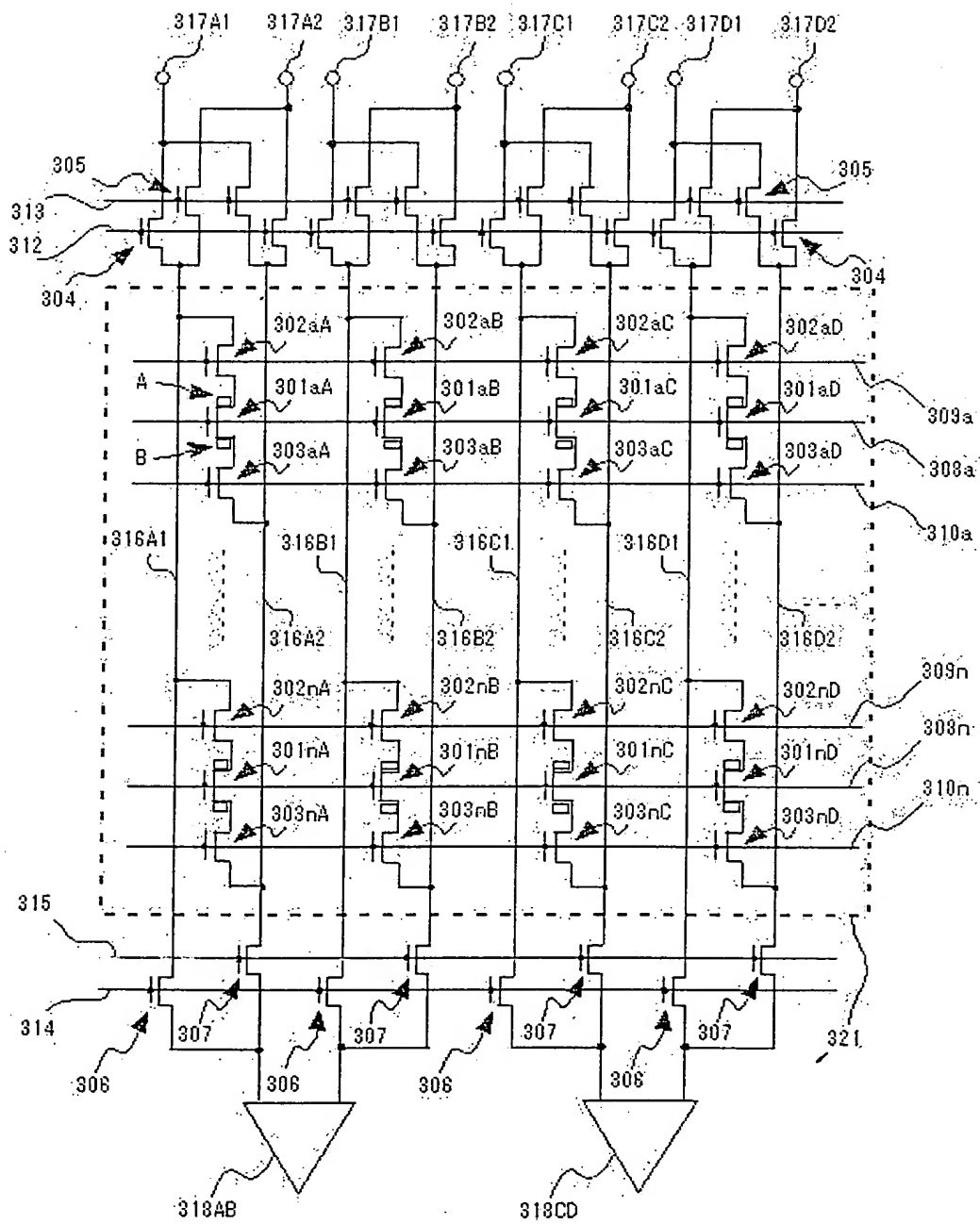
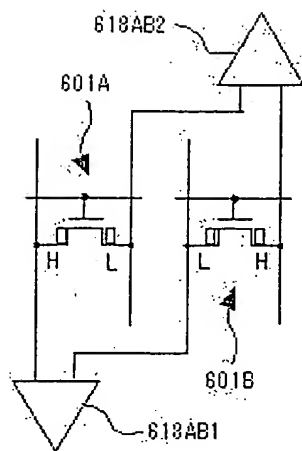
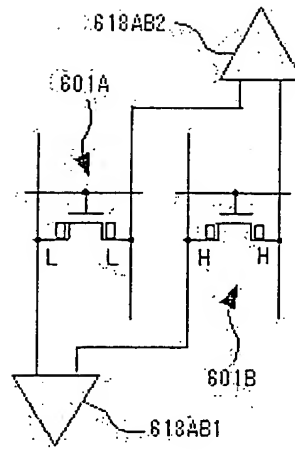


Fig. 20

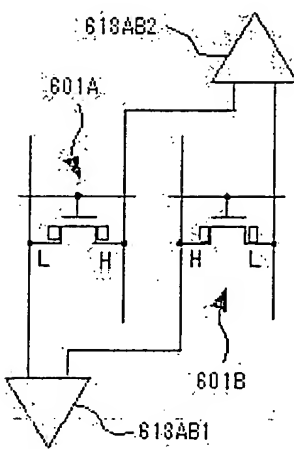




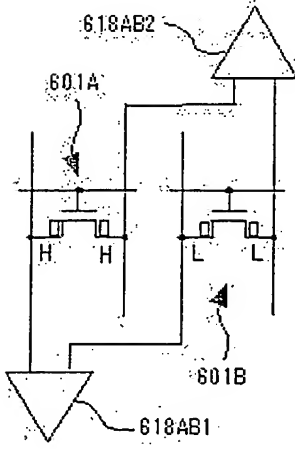
**Fig. 21A**



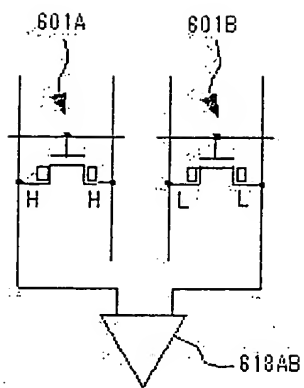
**Fig. 21B**



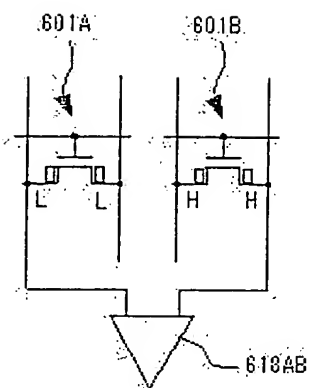
**Fig. 21C**



**Fig. 21D**

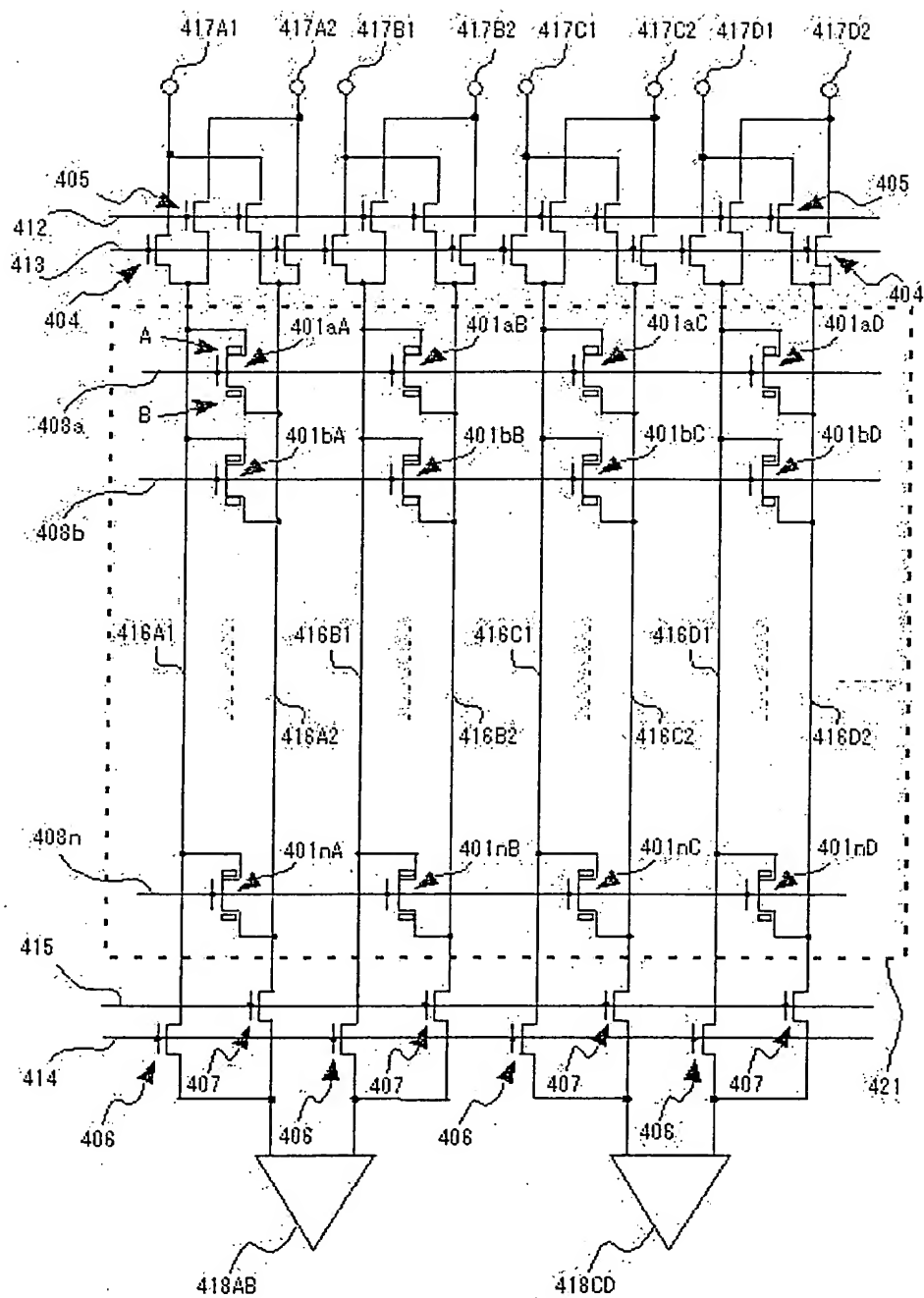


**Fig. 22A**

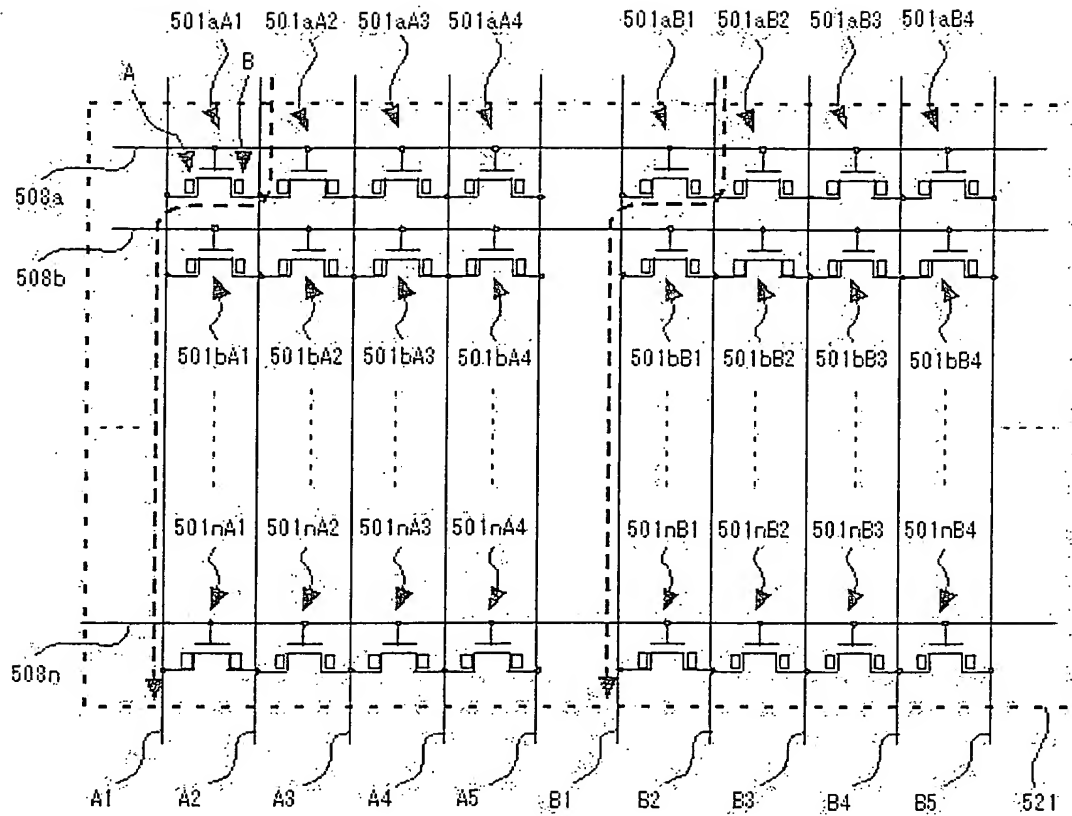


**Fig. 22B**

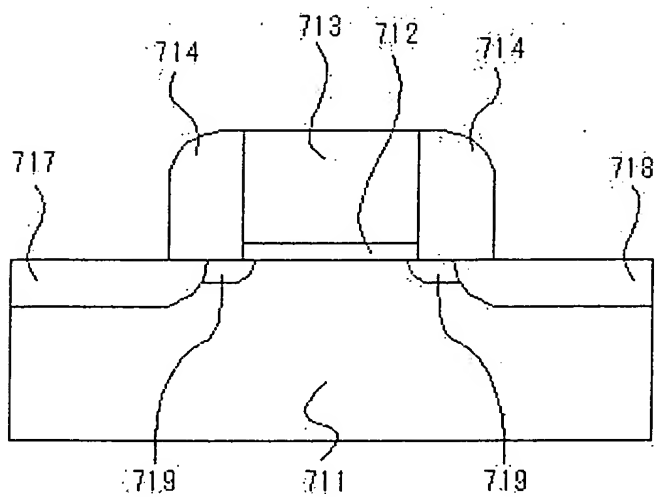
Fig. 23



**Fig. 24**

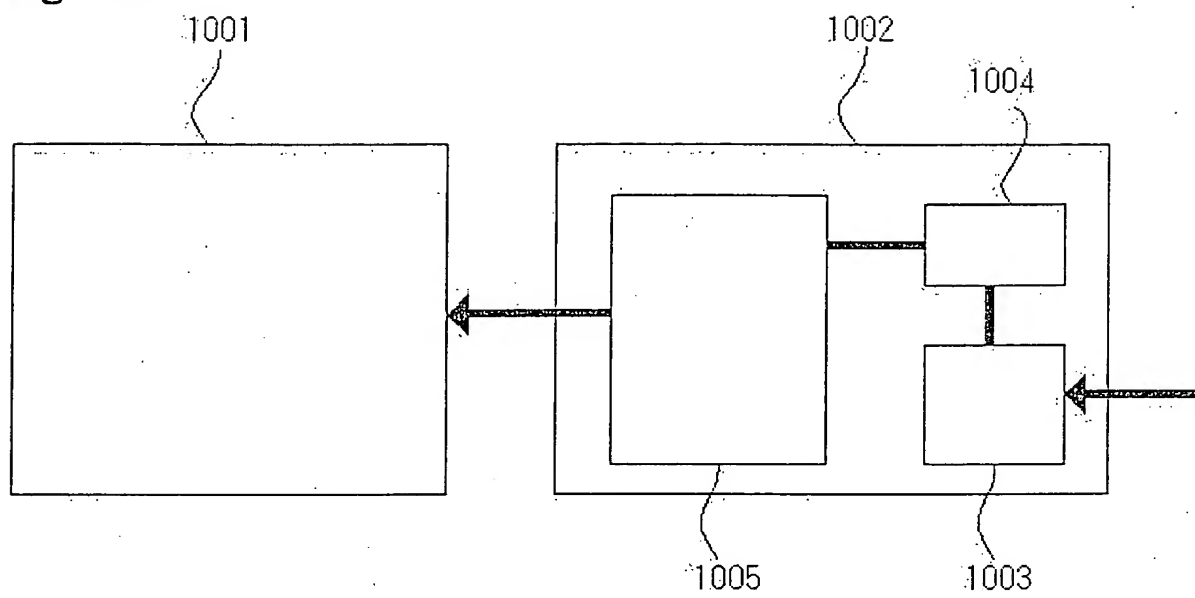


**Fig. 25**

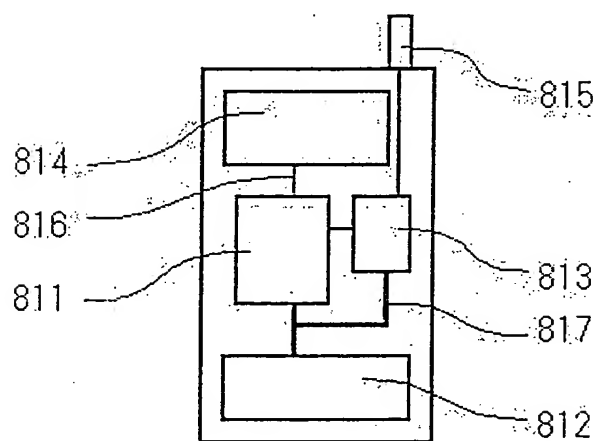


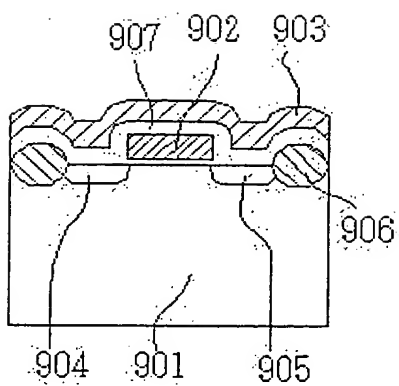


**Fig. 26**

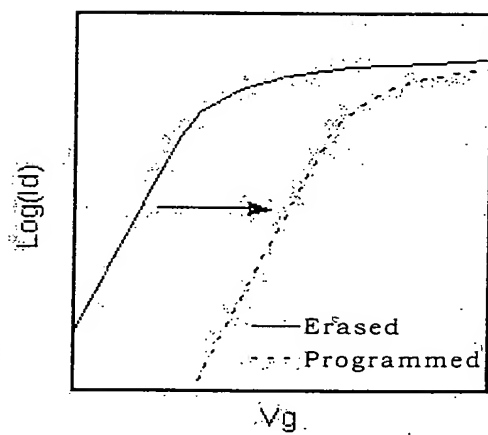


**Fig. 27**





**Fig. 28**  
prior art



**Fig. 29**  
prior art